IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Appln. Of: ITO

Serial No.: 09/735,005

Filed: December 12, 2000

For: SEMICONDUCTOR DEVICE HAVING DUMMY GATES...

Group: 2811

Examiner: GEBREMARIAM, SAMUEL A. DOCKET: NEC 444

MAIL STOP APPEAL BRIEF -- PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER

Dear Sir:

In connection with the above-entitled matter, enclosed please find the following:

1. Three copies of Appellant's Brief on Appeal and Appendix A under Rule 192; and

2. Credit Card Payment Authorization Form PTO-2038 in the amount of $500.00 to cover the cost of filing the Appeal Brief.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,

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By Linda Vanbel

NPS:lv

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APPELLANT'S BRIEF ON APPEAL

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APPELLANT'S BRIEF ON APPEAL

This Brief is being filed in support of Appellant's Appeal From the Final Rejection by the Examiner, the Notice of which was timely filed on October 15, 2004.

REAL PARTY IN INTEREST

The Real Party in Interest in this Appeal is NEC Electronics Corporation, having its principal place of business at 1753 Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa 211-8668, JAPAN. The Application was originally assigned to NEC Corporation by the Inventor, and the Assignment recorded in the U.S. Patent and Trademark Office on December 12, 2002 at Reel 013736, Frame 0321. The Application subsequently was assigned to NEC Electronics Corporation by NEC Corporation, and that Assignment was recorded in the U.S. Patent and Trademark Office on February 19, 2003 at Reel 013736, Frame 0321.

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RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and the belief of the undersigned attorney and Appellant, no appeals or interferences exist that would directly affect, or be directly affected by, or have a bearing on the Board's decision in the instant Appeal.

STATUS OF THE CLAIMS ON APPEAL

Claims 37-40, 42-45, and 47 are pending in the current Application. Claims 1-11 and 24-32 have been withdrawn from consideration pursuant to provisional election in Appellant's Amendment A. Claims 37-40, 42-45 and 47 stand finally rejected and are on Appeal. Claims 37-40, 42-45 and 47 are set forth in **Appendix A** attached hereto.

STATUS OF THE AMENDMENTS

Appellant filed Amendment G under Rule 116 in response to the Examiner's Final Office Action mailed June 16, 2004. Amendment G under Rule 116 cancelled claim 46 and made minor changes to claims 37, 42, and 45 to obviate a §112 rejection. Amendment G under Rule 116 was entered and responded to by the Examiner in the Advisory Action mailed October 6, 2004 ("Advisory Action"). In this Advisory Action, the Examiner withdrew his §112 rejections to claims 42-44, and 47, but not his art rejections of the remaining claims.

BACKGROUND OF THE INVENTION

The Invention on Appeal relates to the manufacture of semiconductor devices. As noted in Appellant's specification, one conventional method used to manufacture a semiconductor device involves depositing a gate conductive layer on a silicon substrate. A photoresist layer is then coated on the gate conductive layer. Next, the photoresist layer is exposed to ultraviolet light via a photomask. The photomask usually has a tight pattern, such

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as a comb-shaped gate pattern, and a coarse pattern such as an isolated gate pattern. The gate is patterned by an etching process using the photoresist layer as a mask. In this method, even if all the gates in the photomask have the same gate length, the gate length of the comb-shaped gate pattern is smaller than the gate length of the isolated pattern of the gate conductive layer. This disparate gate length is caused by the proximity effect, i.e. light diffraction during development of the photomask and the amount of the gate conductive layer redeposited on the sidewalls after the etching process of the gate conductive layer (Specification, page 1, lines 14-37).

In a second conventional method of forming gates, a dummy gate is interposed between the gates, so as to homogenize the proximity effect and the amount of the redeposited gate conductive layer (Specification, page 2, lines 1-5). More particularly as described in the specification in the paragraph bridging pages 9-10, a gate conductive layer is deposited on a monocrystalline silicon substrate. A trench 5' is formed in the area between where the two gates will be formed. Thereafter, the silicon oxide layer 2, and the silicon nitride layer 3 are formed on the gate areas of the gate conductive layer. A CMP process is carried out so that a silicon oxide layer 6 (STI) is buried in the trench 5'. However, in this second conventional method, the STI layer 6 becomes indented and the reliability of the connective wiring is decreased. (See FIG. 9 reproduced below):

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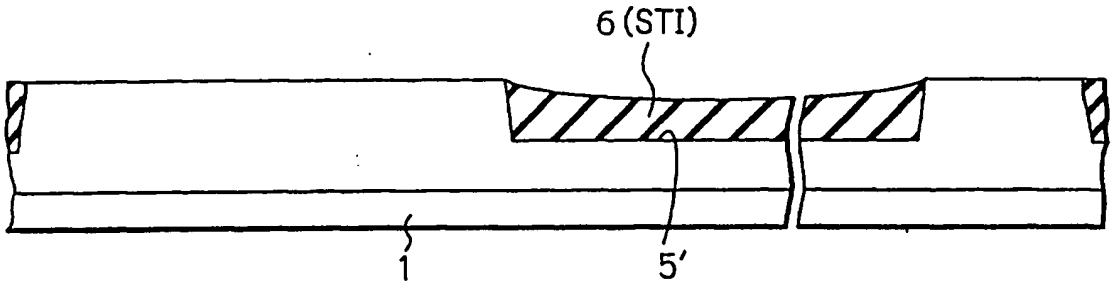
Fig. 9B



Also, additional design time is required if a plurality of kinds of comb-shaped gate patterns are present, which adds significantly to manufacturing cost (Specification, page 2, lines 6-12).

THE INVENTION ON APPEAL

The Invention on Appeal relates to a method for manufacturing a semiconductor device using dummy areas and gates to minimize the proximity effect and overpolishing during the etching process. Specifically, the present invention provides an efficient manufacturing method to insure that lengths of all the gate pattern are equal and formed on level surfaces.

Appellant's manufacturing method involves first creating two photomasks. A first photomask is created with areas containing the gate patterns designated as active areas and the other areas specified as isolation areas. Square dummy patterns are placed within the isolation areas to form the dummy gate pattern areas. The combination of the active areas and the square dummy patterns form the first photomask (Specification, page 6, lines 17-22). The square dummy patterns equalize the distance between elements during etching and thus equalize the gate lengths.

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A second photomask is created by placing dummy gate patterns in the areas corresponding to the square dummy patterns of the first photomask. Each of the dummy gate patterns is a reduction of the corresponding square dummy area. The dummy gate pattern is combined with the gate patterns to form the second photomask used during the manufacturing process (Specification, page 6, line 28 -- page 7, line 5).

Appellant's manufacturing method uses these two photomasks to form a trench structure and overlay the gate pattern on the trench structure. First, a monocrystalline silicon substrate is thermally oxidized to form a silicon oxide layer thereon. A silicon nitride layer is then deposited on the silicon oxide layer and a photoresist layer is coated on the silicon nitride layer. The photoresist layer is irradiated with ultraviolet light via the first photomask. The photoresist layer is developed, so that the photoresist layer is patterned with active areas and the square dummy pattern.

Next, the silicon nitride layer is etched by using the photoresist layer as a mask and the silicon oxide layer as an etching stop. The silicon oxide layer is etched by using the silicon nitride layer as a mask and the photoresist layer is removed (Specification, page 7, line 21 -- page 8, line 13).

Next, a CMP process is carried out to flatten the silicon oxide layer using the silicon nitride layer as a stop. Next, a gate conductive layer made of silicon is deposited. Then, an anti-reflection coating (ARC) layer made of organic material is coated on the gate conductive layer. Then, a photoresist pattern layer is coated on the ARC layer, and is irradiated with ultraviolet light via the second photomask and the photoresist layer is developed (Specification, page 8, lines 28-35).

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Next, the ARC layer and the gate conductive layer are sequentially etched by using the photoresist layer as a mask. Finally, the photoresist layer and the ARC layer are sequentially removed (Specification, page 9, lines 4-8).

With Appellant's process, the lengths of the photoresist comb-shaped gate patterns are equal to the length of the isolated gate pattern and the distortions caused by the proximity effect are minimized.

ISSUE PRESENTED ON APPEAL

The issues presented on Appeal are:

(1) Whether claims 37 and 39-40 are rendered obvious by Admitted Prior Art (APA) in view of Gilbert et al. (US Patent No. 5,885,856).

(2) Whether claim 38 is rendered obvious by Admitted Prior Art (APA) in view of Gilbert et al. (US Patent No. 5,885,856) and in further view of Shimomura et al. (US Patent No. 6,140,687).

(3) Whether claims 42-45 and 47 are rendered obvious by Gilbert et al. (US Patent No. 5,885,856) in view of Admitted Prior Art (APA).

THE FINAL ACTION

In finally rejecting the claims on Appeal, the Examiner states the following:

> 3. **Claims 37 and 39-40 are rejected under 35 USC § 103(a) as being unpatentable over Admitted Prior Art in view of Gilbert et al. US Patent No. 5,885,856.**
>
> "Regarding claim 37 admitted prior art teaches (figs. 3A-3C and 4) a method for manufacturing a semiconductor device comprising the steps of: forming a conductive layer (202) over the semiconductor substrate (201) forming a photoresist pattern layer on the conductive layer using a photomask having gate

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patterns (P1) and (P2) corresponding to the active areas and dummy gate patterns (DP) corresponding to the dummy areas and patterning the conductive layer by an etching process using the photoresist pattern.

Admitted prior art does not disclose forming a first photoresist pattern layer, a first photomask and forming a trench in the semiconductor substrate by an etching process using the first photoresist pattern layer.

It is conventional and well known to form isolation trench using photolithographic process. Gilbert also teaches (fig. 1, col. 2, lines 41-60) forming isolation trench (13) and burying insulating layer in the trenches and using masking layer (12) between active areas (14) and dummy regions (20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first masking process for forming trench isolation trench structure taught by Gilbert in the process of admitted prior art in order to form isolation structures between the active region before forming the gate and dummy gate structures. Furthermore the combined process of admitted prior art and Gilbert results in a structure where each of the dummy gate patterns having a reduced area of the respective one of the dummy area patterns.

Regarding claims 39 and 40 admitted prior art teaches substantially the entire claimed method of claim 37 above except explicitly stating that the dummy areas and or dummy gates are arranged in at least two rows and/or two columns and the row is shifted from another and the row and/or at least one column is shifted from another column.

It is conventional and also taught by Gilbert (fig. 6 and 7) arranging device structures in an array as claimed.

It would well (sic) within ordinary skill in the art to arrange the dummy gate and gate structures of admitted prior art device in the conventional manner in order to obtain high packing density." (Final Action mailed 6/16/04 pgs. 3-5.)

7. **Claim 38 is rejected under 35 USC § 103(a) as being unpatentable over Admitted Prior Art in view of Gilbert et al.**

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US Patent No. 5,885,856 and in further view of Shimomura et al. US Patent No. 6,140,687.

"Regarding claim 38 admitted prior art teaches substantially the entire claimed method of claim 37 above except explicitly stating that the shape of the dummy area and/or dummy gate is a circle.

It is conventional and also taught by Shimomura forming circular shaped gates.

It would be well within ordinary skill in the art to select circular shape dummy/gate structures since circular structures allow for symmetrical arrangement of integrated circuit layout. Furthermore since it is known to form circular shaped gate electrodes it would have been obvious to form circular dummy gate electrode." (Final Action mailed 6/16/04 pg. 5.)

8. **Claims 42-45 and 47 are rejected under 35 USC § 103(a) as being unpatentable over Gilbert et al. US Patent No. 5,885,856 in view of Admitted Prior Art.**

"Regarding claim 42, Gilbert teaches a method of manufacturing a semiconductor device, comprising: performing a selective etching on a semiconductor substrate (11) having first and second active areas (14) and an isolation area (13) intervening between the first and second active areas, thereby forming a grid-shaped trench (13) in the isolation area of the semiconductor substrate to define a plurality of dummy regions (20) each surrounded by the grid-shaped trench; forming an insulating layer (15) in the grid-shaped trench.

Gilbert does not teach forming a conductive layer on the semiconductor substrate; and selectively removing the conductor layer to form a transistor gate over each of the first and second active areas and a dummy gate over each of the dummy regions, the dummy gate having a reduced shape area as compared to a shape area of a corresponding one of said dummy regions.

Admitted prior art teaches (fig. 3A-3C) forming a conductive layer (202) on the semiconductor substrate and selectively removing the conductor layer to form a transistor gate over a first

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and second active areas and a dummy gate (DP) over a dummy regions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transistor and dummy gate structures taught by admitted prior art in the process of Gilbert in order to form an integrated structure with no dishing problem.

Furthermore the combined process of admitted prior art and Gilbert results in a structure where each of the dummy gate patterns having a reduced area of the respective one of the dummy area patterns.

Regarding claim 43, Gilbert teaches substantially the entire claimed process of claim 42 above including the insulating layer is formed by chemical mechanical polishing process (col. 2, lines 41-51).

Regarding claim 44, Gilbert teaches substantially the entire claimed process of claim 42 above including transistor gate and the dummy gate are formed by use of such a mask pattern that is derived by combining a transistor gate pattern and a dummy gate pattern which is obtained by reducing a mask pattern for forming the grid shaped trench.

Regarding claim 45, Gilbert teaches substantially the entire claimed process of claim 42 above including forming two or more dummy gates over the element isolation region between the first and the second gate electrodes (see figs. 3A-3C APA)." (Final Action mailed 6/16/04 pgs. 5-7.)

GROUPING OF CLAIMS

Claims 37 and 39-40 are grouped together as containing the same essential patentable limitations. These claims stand or fall together.

Claim 38 stands alone.

Claims 42-44 are grouped together as containing the same essential patentable limitations. Thus, these claims stand or fall together.

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Claims 45 and 47 are grouped together as containing the same essential patentable limitations. Thus, these claims stand or fall together.

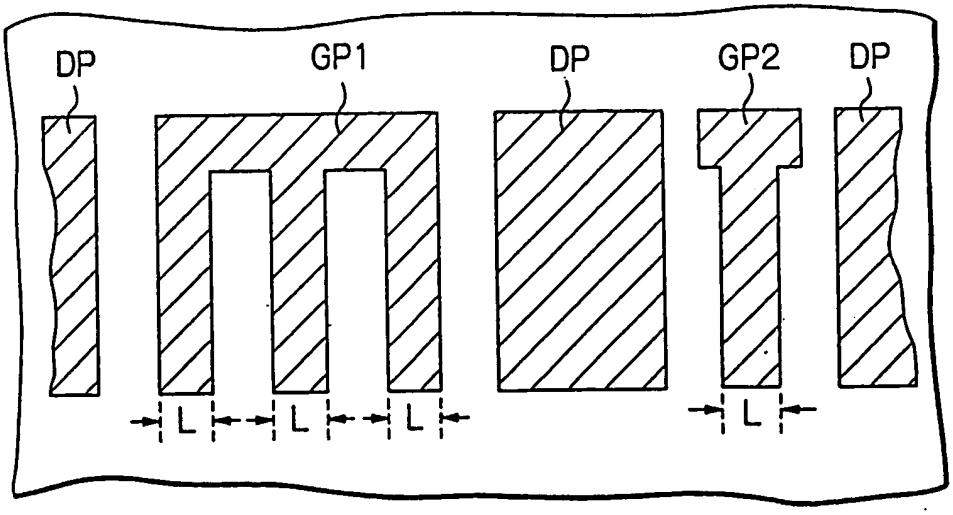
As noted *supra*, the claims on Appeal are set forth in **Appendix A** attached hereto.

THE REFERENCES

Admitted Prior Art ("APA")

The Admitted Prior Art (APA) teaches a method of manufacturing a semiconductor device using dummy gate patterns. In this method, a gate conductive layer and a photoresist layer are deposited on a silicon substrate. Ultraviolet light via a photomask is used to expose the photoresist layer. As shown in FIG. 4, the photomask contains a comb-shaped gate pattern GP1, an isolated gate pattern GP2, and dummy gate patterns DP. The dummy gate patterns are individually placed between the gate patterns in such a way to eliminate the proximity effect. That is, these dummy gate patterns interposed between the gates, leaving specific gaps between the gates and the dummy patterns but otherwise filling the area, as shown in FIG. 4.

Fig. 4 PRIOR ART



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Following the exposure of the photoresist layer, the gate conductive layer is patterned by an etching process using the photoresist layer as a mask. Finally, the photoresist layer is removed, leaving gate patterns G1, G2, and dummy gates DG on the semiconductor substrate.

APA's method reportedly eliminates the proximity effect but dramatically increases the design time of the semiconductor device. More particularly, extra time is required to design and place the dummy gates on the semiconductor device. Thus, an unreasonable increase in the turnaround time and design costs results.

Gilbert et al., U.S. Patent No. 5,885,856 ("Gilbert et al.")

Gilbert et al. teaches adding dummy structures to the layout pattern of an integrated circuit. The location of each dummy structure is predetermined so as not to intersect a well boundary or an active region and not to fall under a layer of a conductive material or an interconnected structure. (Abstract.)

Gilbert et al. also teaches forming trenches between various mesa structures and dummy areas. To form these trench structures, Gilbert et al. teaches a masking layer such as silicon nitride, is formed on the surface of semiconductor substrate. A photolithographic pattern is then formed on masking layer, and a reactive ion etch (RIE) is used to form trench structures using the photolithographic pattern as an RIE etch mask. Trench structures are then filled with a non-conductive material to provide the necessary electrical isolation within the trenches. Polishing is then used to remove the excess portions of the non-conductive material, which overlie a top opening of the trenches. (Col. 2, line 41 -- col. 3, line 63).

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Shimomura et al., U.S. Patent No. 6,140,687 ("Shimomura et al.")

According to Shimomura et al., an active area surrounded with an isolation is formed on a silicon substrate, a large number of unit cells are disposed in a matrix, and the unit cell together form one MOSFET. Each of the unit includes a ring gate electrode in the shape of a regular octagon, a drain region and a source region formed at the inside and outside of the gate electrode, respectively, two gate withdrawn wires extending from the gate electrode to area above the isolation, a substrate contact portion in which the surface of the substrate is exposed, and contacts for electrically connecting these elements with wires. These elements such as the ring gate electrode and the gate withdrawn wires are formed so as to attain a high frequency characteristic as good as possible. (Abstract).

ARGUMENTS ON APPEAL

I. THE REJECTION OF CLAIMS 37, 39-40, 42-45 AND 47 AS BEING UNPATENTABLE OVER THE COMBINATION OF APA AND GILBERT ET AL. IS IMPROPER BECAUSE NO COMBINATION OF APA AND GILBERT ET AL. DOES NOT TEACH OR RENDER OBVIOUS APPELLANT'S INVENTION.

1. APA and Gilbert et al. do not teach dummy gate patterns having a smaller area than the dummy area patterns as required by independent claims 37 and 42.

Independent claim 37 requires "[e]ach of said dummy gate patterns having a reduced area of a respective one of said dummy area patterns"; and, independent claim 42 requires "[d]ummy gates having a reduced shape area as compared to a shape area of a corresponding one of said dummy regions." Thus, according to Appellant's claimed invention each of the dummy gate patterns 9(DP) must be smaller than the dummy area pattern below it, i.e. as shown in FIG. 8J below.

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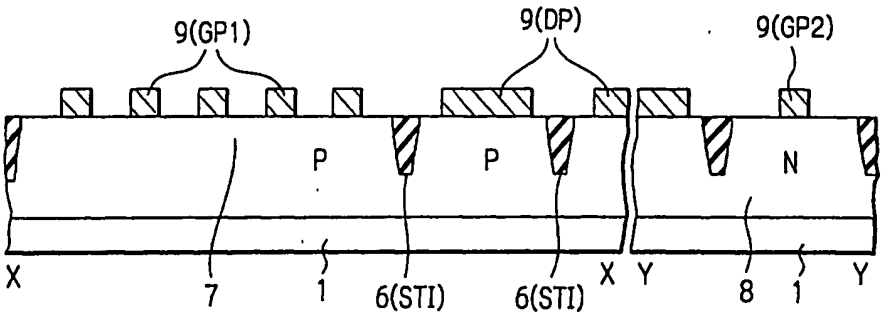
Fig. 8J



The Examiner posits, without any support or citation from either reference, that the combination of APA and Gilbert et al. teach this element. Final Action, dated 06/16/2004, cipher 8 page 6. However, the APA teaches filling area between the gates with dummy gates. The distance between the gate patterns and the dummy gate patterns is set such that the proximity effect is homogenized in the gate pattern and all the gates have an equal length.

Gilbert et al. surrounds the gate areas with a pattern of dummy structures. Trenches separate the dummy structures from the gate areas. The trench length in Gilbert et al. is set such that the polishing rate of the non-conductive metal is equalized everywhere on the substrate.

Thus, placing the gate patterns taught by the APA on Gilbert's semiconductor device, as the Examiner dictates, would not create a semiconductor device with dummy gate patterns smaller than dummy area patterns. Rather, it would create a device where the area of the dummy gate is independent of the dummy area patterns. The area of the dummy gate patterns would be set to eliminate the proximity effect and the dummy area patterns set to equalize

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polishing rates. However, since in the APA the dummy gates fill most of the area between the actual gates, the dummy gates would not be smaller than the dummy area patterns. The Examiner is employing impermissible hindsight reasoning in concluding a reduced area of the dummy gate patterns relative to the dummy area patterns would result. Thus, no combination of APA and Gilbert et al. would achieve or render obvious independent claims 37 and 42, or any of the claims dependent thereon, and the rejection is in error.

2. The combination of APA and Gilbert et al. fail to teach removing the first photoresist pattern layer before depositing the trench insulating layers as required by claim 37.

Appellant's independent claim 37 requires "[b]urying insulating layers in said trenches after first photoresist pattern layer is removed." As the Examiner admits, APA does not teach forming a first photoresist pattern layer or a trench. Final Action, dated 06/16/2004, cipher 6, page 4. Gilbert et al. does not provide the missing teaching of removing the first photoresist before depositing the trench insulating layer. Gilbert teaches:

> "a masking layer such as silicon nitride, is formed on the surface of semiconductor substrate. A photolithographic pattern is then formed on masking layer, and a reactive ion etch (RIE) is used to form trench structures using the photolithographic pattern as an RIE etch mask. Trench structures are then filled with a non-conductive material...to provide the necessary electrical isolation within the trenches."

Nowhere does Gilbert et al. teach removing the first photoresist layer. Thus, no combination of APA and Gilbert et al. can achieve or render obvious Appellant's independent claim 37 or any of the claims dependent thereon, and the rejection is in error.

3. The requirement of independent claim 45 of forming two or more dummy gates on the isolation region is not taught by APA and Gilbert et al.

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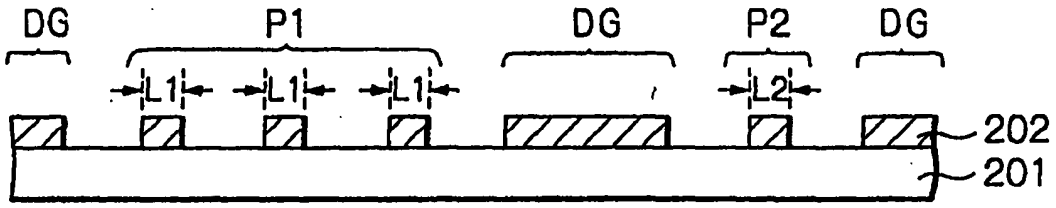
Appellant's independent claim 45 requires "[f]orming two or more dummy gates over said element isolation region between said first and second gate electrodes." As shown in FIG. 3C, the APA teaches one large dummy gate in the isolation region. Furthermore, it would not be obvious to form two or more dummy gates based on the APA. Forming two or more dummy gates would increase the cost and complexity of designing the semiconductor device with no apparent benefit based on the teachings of the APA.

Fig. 3C PRIOR ART



Gilbert does not provide the missing teaching. As the Examiner admits, Gilbert et al. does not teach forming dummy gates over the isolation regions. Final Action, dated 06/16/2004, cipher 8 page 6. Therefore, the combination of APA and Gilbert et al. do not achieve nor render obvious independent claim 45 or any of the claims dependent thereon, and the rejection is in error.

II. THE REJECTION OF CLAIM 38 AS UNPATENTABLE OVER APA IN VIEW OF GILBERT ET AL. AND FURTHER IN VIEW OF SHIMOMURA ET AL. IS IMPROPER BECAUSE THE COMBINATION OF APA, GILBERT ET AL. DOES NOT TEACH OR RENDER OBVIOUS APPELLANT'S EVERY ELEMENT OF CLAIM 38.

Claim 38 depends on independent claim 37. The deficiencies of the APA and Gilbert et al. vis-à-vis independent claim 37 are discussed above. Shimomura et al. does not supply the

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missing teaching of APA and Gilbert et al. to achieve or render obvious independent claim 37 or claim 38, which depends thereon. Shimomura has been cited as teaching the shape of the dummy gates are circular. Detail Action, dated 06/16/2004, cipher 7 page 5. However, Shimomura et al. teaches gates in the shape of regular octagons, not circles. But, even assuming *arguendo* the Examiner's characterization of Shimomura et al., the more basic teachings required by independent claim 37, as discussed above, are not supplied by Shimomura et al. Thus, no combination of APA, Gilbert et al., and Shimomura et al. would achieve or render obvious claim 38, and the rejection is in error.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner's Final Rejection of the subject Application is in error, and it is requested that the Rejection be reversed in all respects.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP APPEAL BRIEF-PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 15, 2004, at Tucson, Arizona.

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APPENDIX A

Serial No. 09/735,005
Docket No. NEC 444

CLAIMS ON APPEAL
filed with
APPELLANT'S BRIEF

APPENDIX A

CLAIMS ON APPEAL:

Claim 37: A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

forming, on said semiconductor substrate, a first photoresist pattern layer using a first photomask having active area patterns corresponding to active areas and dummy area patterns corresponding to dummy areas;

forming a trench in said semiconductor substrate, which trench partitions pattern areas corresponding to said dummy area patterns from pattern areas corresponding to said active area patterns, by an etching process using said first photoresist pattern layer as an etching mask;

removing said first photoresist pattern layer;

burying insulating layers in said trenches after said first photoresist pattern layer is removed;

forming a conductive layer on said semiconductor substrate;

forming a second photoresist pattern layer on said conductive layer using a second photomask having gate patterns corresponding to said active areas and dummy gate patterns corresponding to said dummy areas; and

patterning said conductive layer by an etching process using said second photoresist pattern layer, each of said dummy gate patterns having a reduced area of a respective one of said dummy area patterns.

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Claim 38: The method as claimed in claim 37, wherein the shape of at least one said dummy area patterns and/or dummy gate patterns is a circle.

Claim 39: The method as claimed in claim 37, wherein a plurality of said dummy area patterns and/or dummy gate patterns are arranged in at least two rows and/or two columns.

Claim 40: The method as claimed in claim 39, wherein at least one said row is shifted from another said row and/or at least one column is shifted from another said column.

Claim 42: A method of manufacturing a semiconductor device, comprising:

performing a selective etching on a semiconductor substrate having first and second active areas and an isolation area intervening between said first and second active areas, thereby forming a grid-shaped trench in said isolation area of said semiconductor substrate to define a plurality of dummy regions each surrounded by said grid-shaped trench;

forming an insulating layer in said grid-shaped trench;

forming a conductive layer on said semiconductor substrate; and

selectively removing said conductive layer to form a transistor gate over each of said first and second active areas and a dummy gate over each of said dummy regions, said dummy gate having a reduced shape area as compared to a shape area of a corresponding one of said dummy regions.

Claim 43: The method as set forth in claim 42, wherein said insulating layer is formed by chemical mechanical polishing process.

Claim 44: The method as set forth in claim 42, wherein said transistor gate and said dummy gate are formed by use of such a mask pattern that is derived by combining a transistor

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gate pattern and a dummy gate pattern which is obtained by reducing a mask pattern for forming said grid-shaped trench.

Claim 45: A method of manufacturing a semiconductor device, comprising:

defining in a semiconductor substrate first and second element formation regions and an element isolation region isolating said first and second element formation regions from each other;

forming first and second gate electrodes over said first and second element formation regions, respectively; and

forming two or more dummy gates over said element isolation region between said first and second gate electrodes.

Claim 47: The method as claimed in claim 45, wherein each of said dummy gates has a shape that is reduced as compared to said portion of said element isolation region.

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